AND8322

Four Key Steps to Design a Continuous Conduction Mode PFC Stage Using the NCP1654

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This paper proposes the key steps to rapidly design a Continuous Conduction Mode (CCM) PFC stage driven by the NCP1654. The process is illustrated by the following practical application:

– Maximum output power: 300 W

– Input voltage range: from 85 Vrms to 265 Vrms

– Regulation output voltage: 390 V

– Switching frequency: 65 kHz

INTRODUCTION

The NCP1654 is a controller for Continuous Conduction Mode (CCM) Power Factor Correction step−up pre−converters. It controls the power switch conduction time (PWM) in a fixed frequency mode and in dependence on the instantaneous coil current.

Housed in a SO8 package, the circuit minimizes the number of external components and drastically simplifies the PFC implementation. It also integrates high safety protection features that make the NCP1654 a driver for robust and compact PFC stages like an effective input power runaway clamping circuitry.

Generally, the NCP1654 is an ideal candidate in systems where cost−effectiveness, reliability and high power factor are the key parameters. It incorporates all the necessary features to build a compact and rugged PFC stage:

- **Compactness and Flexibility:** Easy to implement, the NCP1654 yields near−unity power factor in a simple and robust manner. Despite the low external components count it requires, the circuit sacrifices neither performance nor flexibility. Instead, by simply adjusting an external resistor, you can even choose to have the circuit operated in traditional or follower boost mode (Note 1).
- **Low Consumption and shutdown Capability:** The NCP1654 particularly, minimizes its consumption during the startup phase and in shutdown mode. Hence, the PFC stage losses are extremely low when the circuit is off. This feature helps meet the more stringent standby low power specifications. Grounding the Feedback pin (pin 6) forces the NCP1654 in shutdown mode.
- **Safety Protections:** The NCP1654 permanently monitors the input and output voltages, the coil current and the die temperature to protect the system from possible over−stresses. More specifically, the following protections make the PFC stage extremely robust and reliable:

– Maximum Current Limit: The circuit immediately turns off the MOSFET if the coil current exceeds the maximum permissible level. The NCP1654 also prevents any turn on of the power switch as long as the coil currents is not below this limit. This feature protects the PFC stage during the startup phase when large in−rush currents charge the output capacitor.

– Under Voltage Protection/Shutdown: The circuit keeps in shutdown mode as long as the feedback voltage indicates that the output voltage is lower than 8% its regulation level. In this case, the NCP1654 consumption is very low (<400 μA). This feature protects the PFC stage from starting operation in case of a failure in the feedback network (e.g., bad connection).

– Brown−Out Detection: The circuit detects the AC line voltage via the resistor divider. In case of too low AC line conditions, the circuit keeps in shutdown mode.

– Over Voltage Protection: Given the low bandwidth of the regulation block, PFC stages may exhibit dangerous output voltage overshoots because of abrupt load or input voltage variations (e.g. at startup). Over Voltage Protection (OVP) turns off the Power Switch as soon as V_{out} exceeds the OVP threshold (105% of the regulation level).

– Over Power Limitation: The NCP1654 senses the coil current and the input voltage and based on these information, the circuit is able to detect excessive power levels. In this case, it turns off the MOSFET.

– Thermal Shutdown: An internal thermal circuitry forces the power switch off when the junction temperature exceeds 150°C typically. The circuit resumes operation once the temperature drops below about 120°C (30°C hysteresis).

1. The “Follower Boost” mode makes the pre−converter output voltage stabilize at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the difference between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage (refer to MC33260 and NCP1654 datasheet at www.onsemi.com)

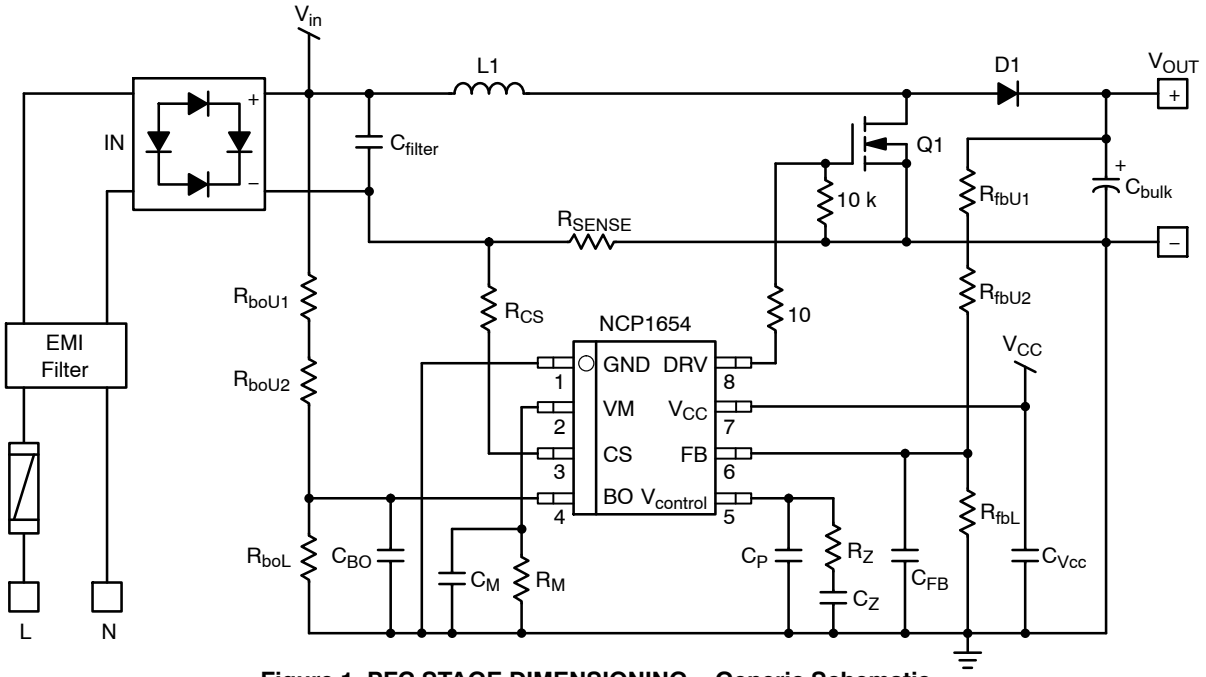

Figure 1. PFC STAGE DIMENSIONING − Generic Schematic

Step 1: Power Components Selection

Basically, the coil, the bulk capacitor and the power silicon devices are dimensioned "as usually", that is, as done with any other CCM PFC. This section does not detail this process, but simply states some key points.

1. Coil Selection

One generally selects the coil to limit the current ripple below a certain pre−determined level, for instance ±15% when the input current is maximum.

The input current amplitude, I_{in}, is maximum at low line and high power. Hence,

$$I_{in,max} = \frac{\sqrt{2}\,P_{out,max}}{\eta \cdot V_{acLL}} \qquad \text{(eq. 1)}$$

where $P_{out,max}$ is the maximum output power, η the efficiency and V_{acLL} the AC line lowest level.

Consequently, if we assume a 92% efficiency, our 300 W application leads to the following maximum AC line peak current:

$$\sqrt{2} \cdot 300 \,/\, (0.92 \cdot 85)$$

that is 5.4 A.

On the other hand, one could show that at the sinusoid top, the peak−to−peak ripple of the coil current, is given by the following equation:

$$\frac{\sqrt{2}\,V_{ac}}{L \cdot f_{sw}}\left(1 - \frac{\sqrt{2}\,V_{ac}}{V_{out}}\right) \qquad \text{(eq. 2)}$$

where f_{sw} is the operating frequency. Typically, one targets the peak−to−peak ripple between 10 and 50% of the AC line current maximum amplitude, $I_{in,max}$.

Therefore if we target a ±18% ripple at low line, i.e. $I_{coil,pp}$ is 36%, the coil inductance, L, is given by the following equation:

$$\frac{\sqrt{2}\,V_{acLL}}{L \cdot f_{sw}}\left(1 - \frac{\sqrt{2}\,V_{acLL}}{V_{out}}\right) = 36\%\,\frac{\sqrt{2}\,P_{out,max}}{\eta \cdot V_{acLL}} \qquad \text{(eq. 3)}$$

Hence, the coil inductance is:

$$L = \frac{\eta \cdot V_{acLL}^{\,2}}{0.36 \cdot f_{sw} \cdot P_{out,max}}\left(1 - \frac{\sqrt{2}\,V_{acLL}}{V_{out}}\right) \qquad \text{(eq. 4)}$$

The combination of 390 V for the output voltage (V_{out}) and 65 kHz for the switching frequency, leads to a coil inductance in the range of 655 μH. In practice, we have chosen 650 μH that more specifically, leads to about a 36% peak−to−peak ripple.

Finally, if one neglects the switching ripple of the coil current, its rms value equates the rms AC line current. In other words:

$$I_{coil,rms} = \frac{P_{out}}{\eta \cdot V_{ac}} \qquad \text{(eq. 5)}$$

The maximum RMS current of the coil is then:

$$I_{coil,rms,max} = \frac{P_{out,max}}{\eta \cdot V_{acLL}} \qquad \text{(eq. 6)}$$

The coil specification is then:

- L = 650 μH
- $I_{coil,max}$ = 6.4 A (maximum amplitude of the AC line current + ripple)
- $I_{coil,rms}$ = 3.8 A

2. Power Silicon Devices

Generally, the diode bridge, the power MOSFET and the output diode will be placed on the same heatsink.

As a rule of the thumb, one can estimate that the heatsink will have to dissipate around:

- 6% of the output power in wide mains applications (92% being generally the targeted minimum efficiency)
- 3% of the output power in European mains applications

Among the sources of losses that contribute to this heating, one can list:

- The diodes bridge conduction losses that can be estimated by the following equation:

$$P_{bridge} = \frac{4\sqrt{2}}{\pi}\frac{V_f}{V_{acLL}}\frac{P_{out}}{\eta} \approx 1.8\frac{V_f}{V_{acLL}}\frac{P_{out}}{\eta} \quad \text{(eq. 7)}$$

where V_f is the forward voltage of the ridge diodes.

- The MOSFET conduction losses, that if one neglects the current ripple, are given by:

$$P_{on,max} = R_{DS(on)} \cdot \left(\frac{P_{in,max}}{V_{acLL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2}V_{acLL}}{3\pi V_{out}}\right) \quad \text{(eq. 8)}$$

- The output diode conduction losses: ($I_{out} \cdot V_f$), where I_{out} is the load current and V_f is the diode forward voltage. The maximum output current being nearly 0.77 A (= 300 W / 390 V), the diode conduction losses are in the range of 0.77 W (assuming V_f = 1.0 V).

In our case, we have:

- P_{bridge} = 6.9 W, assuming that V_f is 1.0 V.
- $P_{on,max} = 10.8 \cdot R_{DS(on)}$. In our application, a low $R_{DS(on)}$ MOSFET (0.19 Ω) is implemented to avoid excessive MOSFET losses. Assuming that $R_{DS(on)}$ doubles at the high temperatures, the maximum conduction losses are about 4.1 W.
- P_{diode} = 0.77 W.

The diode and MOSFET switching losses are highly dependent on the diode choice, on the MOSFET drive speed and on the possible presence of some snubbering circuitry. Hence, their prediction is a tough and inaccurate exercise that will not be made in this paper.

Instead, they are just assumed to be part of the power budget initially specified for the heatsink (6% of P_{out} in our case). Experimental tests will ensure that the estimation is correct.

3. Output Bulk Capacitor

The bulk capacitance had to satisfy two requirements, which are the output double line frequency ripple and hold−up time.

Output Voltage Ripple Requirement:

The bulk capacitance always presents the voltage ripple of double line frequency (100 or 120 Hz ripple exhibited by the bulk voltage (Note 2).

The voltage ripple constraint requires that

$$C_{bulk} > \frac{P_{out}}{\delta V_{pp,max} \cdot \omega \cdot V_{out}} \quad \text{(eq. 9)}$$

where $\delta V_{pp,max}$ is the maximum permissible peak−to−peak voltage ripple and ω is the AC line angular frequency.

In the NCP1654, Over Voltage Protection (OVP) is 105% of regulation level, which tolerance is from 103% to 107%. This function should be activated only during load or line change. To avoid OVP from being activated in normal operation, the voltage ripple on the bulk capacitor should be chosen below ± 3% ($\delta V_{pp,max}$ = 6% V_{out}). This requirement leads to the following bulk capacitance:

$$C_{bulk} > \frac{300}{6\% \cdot 100\pi \cdot 390^2} \approx 105\ \mu F \quad \text{(eq. 10)}$$

Hold−upTime Requirement:

If some hold−time requirement was specified, this would lead to the following additional constraint:

$$C_{bulk} > \frac{2P_{out} \cdot t_{HOLD}}{V_{out1}{}^2 - V_{out2}{}^2}$$

where V_{out1} is the nominal output voltage (390 V in this case), V_{out2} is the minimum acceptable level of V_{out}, and t_{HOLD} is the hold−up time. For example, t_{HOLD} = 20 ms and V_{out2} = 250 V lead to C_{bulk} > 134 μF.

The C_{bulk} capacitance should be higher than the calculated value from above two requirements. Considering the tolerance of capacitance, 180 μF is chosen here.

Bulk Capacitor Heating:

It must also be checked that the ESR is low enough to prevent the rms current that flows through it, from overheating the bulk capacitor. This rms current depending on the input impedance of the downstream converter, is not computed here.

Step 2: Feedback Arrangement

As shown by Figure 1, the feedback arrangement consists of:

- C_{FB}, a filtering capacitor to avoid that some switching noise may be injected into FB pin. A capacitor ranging from 100 pF to 1 nF is traditionally implemented.
- R_{fbU1}, R_{fbU2}, and R_{fbL} set output voltage. In practice, one generally implements more resistors as upper side feedback loop for safety consideration. Refer to Figure 1, given that V_{out} is a high voltage, an accidental shortage of the feedback resistor would destroy the controller. That is why it is better to have several series resistors instead of only one.

2. The input current and voltage being sinusoidal, PFC stages deliver a squared sinusoidal power that matches the load power demand in average only. When the power fed to the load is lower than the load demand, the output capacitor discharges while it charges when the supplied power exceeds the load consumption. As a consequence, the output voltage exhibits a ripple (e.g., 100 Hz ripple in Europe or 120 Hz in USA) that is inherent to the PFC function.

First, choose the value of the lower resistor, R_{fbL}. There is a trade−off between the noise immunity and the power losses when choosing R_{fbL}. In this application, we select 23.2 kΩ as R_{fbL} that leads a 108 μA feedback current and 42 mW losses. The value of upper resistor R_{fbU} is then given by

$$R_{fbU} = \frac{V_{out} - V_{REF}}{V_{REF}} R_{fbL} \quad \text{(eq. 11)}$$

where:

- V_{REF} is the internal reference voltage for V_{out} feedback (2.5 V typical).
- $R_{fbU} = R_{fbU1} + R_{fbU2}$ is the total feedback resistor placed between V_{out} and FB pin.

In this case, Vout is 390 V and R_{fbL} is 23.2 kΩ, one must then select the following R_{fbU} resistance:

$$R_{fbU} = \frac{390 - 2.5}{2.5} \cdot 23.2\ k\Omega = 3.596\ M\Omega \quad \text{(eq. 12)}$$

One can approximately obtain 3.596 MΩ resistance by implementing: $R_{fbU1} = R_{fbU2} = 1.8$ MΩ. These normalized values precisely give $R_{fbU} = 3.6$ MΩ, that is: 390 V as the regulation level.

- C_P, C_Z, and R_Z connected to $V_{control}$ pin acts as a type−2 compensation loop to set the regulation bandwidth (Note 3). It is recommended to set the bandwidth below 20 Hz for an effective filtering of the 100 or 120 Hz ripple. If C_Z is >> C_P, the transformer of V_{out} to $V_{control}$ is

$$\frac{V_{control}}{V_{out}} = \frac{R_{fbL} \cdot G_{EA} R_Z}{R_{fbL} + R_{fbU}} \cdot \frac{1 + sR_ZC_Z}{sR_ZC_Z(1 + sR_ZC_P)} \quad \text{(eq. 13)}$$

where G_{EA} is the error amplifier gain. Then this comp−ensation provides one original pole, one low frequency zero

$$f_Z = \frac{1}{2\pi \cdot R_Z \cdot C_Z}$$

and one high frequency pole

$$f_P = \frac{1}{2\pi \cdot R_Z \cdot C_P}$$

In this application, we choose $C_P = 0.22$ μF, $C_Z = 2.2$ μF, and $R_Z = 12$ kΩ, which leads to one zero at 6 Hz and one pole at 329 Hz.

Finally:

R_{fbU1}	R_{fbU2}	R_{fbL}	C_{FB}
3.6 MΩ	3.6 MΩ	23.2 kΩ	100 pF
C_P	C_Z	R_Z	
0.22 μF	2.2 μF	12 kΩ	

Step 3: Input Voltage Sensing

Refer to Figure 2, the NCP1654 monitors the input voltage, V_{in}, which is the rectified AC line sinusoid for brown−out, over−power limitation (OPL), and PFC duty cycle modulation. This sensing circuit consists of:

- R_{boU} (= $R_{boU1} + R_{boU2}$ in Figure 1) and R_{boL} are dimensioned to adjust the threshold of brown out protection. Because of the safety consideration, it is recommended to split this upper side brown out resistor into 2 or more resistors.
- C_{BO} that forms a low pass filtering together with R_{boL} to get the average value of input signal. A time constant in the range of around 5 times the V_{in} period should be targeted to make V_{bo} substantially constant and proportional to the mean input voltage as the rule of thumb:

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} < V_{in} > \quad \text{(eq. 14)}$$

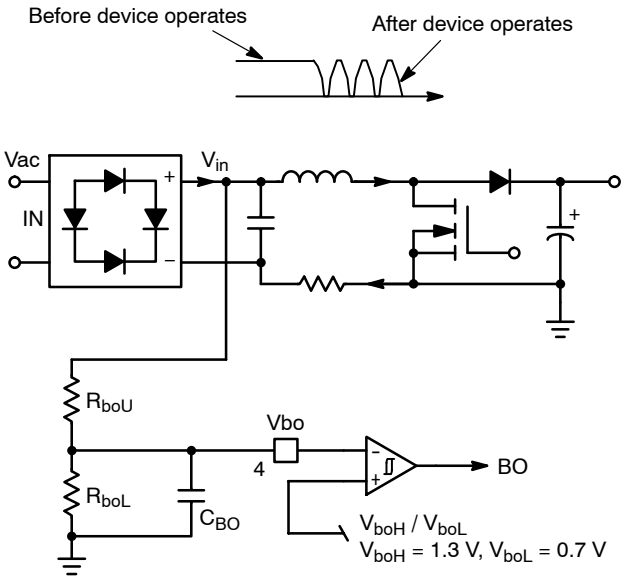

Figure 2. Brown−Out Protection

The NCP1654 starts to operate as V_{bo} exceeds 1.3 V and keeps operating until V_{BO} goes below 0.7 V. The 600 mV hysteresis prevents the system from oscillating. As shown in Figure 2, before the device operates, V_{in} is kept at peak value of the input ac line sinusoid, V_{ac}, that is,

$\sqrt{2}V_{ac}$, which leads to:

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} < V_{in} > = \frac{R_{boL}}{R_{boL} + R_{boU}} \sqrt{2} V_{ac} \quad \text{(eq. 15)}$$

After the device operates, V_{in} is the rectified sinusoidal input voltage, which average value becomes

$\frac{2\sqrt{2}}{\pi}V_{ac}$, which leads to:

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} \frac{2\sqrt{2}}{\pi} V_{ac} \quad \text{(eq. 16)}$$

3. Regarding how to design the compensation in NCP1654, please refer to application note: AND8321, “Compensation of a PFC stage driven by the NCP1654/5”, in www.onsemi.com or the book “Switch−Mode Power Supplies: SPICE Simulations and Practical Designs” written by Christophe Basso.

First, select R_{boL}. R_{boL} should be relatively high impedance to limit the current within R_{boL} and R_{boL} and the associated losses. Please note however that given the bias current of the brown−out comparator (0.5 μA maximum), it is recommended to set the current flowing through R_{boU} and R_{boL} to be in the range or higher than 5 μA at low line. In this application, we use 82.5 kΩ for R_{fbL}, which leads to a bias current of:

$$\frac{0.7\ V}{82.5\ k} = 8.5\ \mu A$$

Second, select R_{boU} according to $V_{ac,on}$, the minimum AC input voltage to start PFC, which comes from (eq. 15):

$$R_{boU} = \frac{\sqrt{2}V_{ac,on} - V_{BOH}}{V_{BOH}}R_{boL} \qquad \text{(eq. 17)}$$

In this application, 75 Vac is targeted as $V_{ac,on}$. Hence,

$$R_{boU} = \frac{\sqrt{2} \cdot 75\ V - 1.3\ V}{1.3\ V} \cdot 82.5\ k\Omega \approx 6.65\ M\Omega$$

Here R_{boU} is split into 2 parts, R_{boU1} and R_{boU2} both equal to 3.3 MΩ for a global 6.6 MΩ resistance.

Third, select C_{BO} to make the time constant be around 5 times T_{Vin}, the cycle time of V_{in} by

$$C_{BO} \approx \frac{5 \cdot T_{Vin}}{R_{boL}} \qquad \text{(eq. 18)}$$

Where T_{Vin} is the duration of an input voltage cycle, that is, half the line period.

In this application, T_{Vin} is 10 ms since the ac input line is 50 Hz. So

$$C_{BO} \approx \frac{5 \cdot 10\ ms}{82.5\ k\Omega} = 0.6\ \mu F$$

Here 0.47 μF is selected because it is the closest normalized value.

Fourthly, check $V_{ac,off}$, the PFC brown−out off threshold of AC input voltage. As shown in Figure 3, because of the ripple voltage on V_{bo}, the minimum value of V_{bo} is around

$$V_{bo} = K_{BO} \cdot \frac{2\sqrt{2}}{\pi}V_{ac} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right) \qquad \text{(eq. 19)}$$

Where

K_{BO} is the scaling down factor of the BO network:

$$K_{BO} = \frac{R_{boL}}{R_{boU} + R_{boL}}$$

f_{BO} is the corner frequency of the BO filter:

$$f_{BO} = \frac{R_{boL} + R_{boU}}{2\pi \cdot R_{boL} \cdot R_{boU} \cdot C_{BO}}$$

f_{line} is the line frequency, i.e. 50 Hz or 60 Hz.

The brown−out function turning off the device is when (eq.19) equal to V_{BOL}, the threshold voltage of brown out comparator, which leads to:

$$K_{BO} \cdot \frac{2\sqrt{2}}{\pi}V_{ac,off} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right) = V_{BOL} \qquad \text{(eq. 20)}$$

Hence we can get

$$V_{ac,off} = \frac{V_{BOL}}{K_{BO} \cdot \frac{2\sqrt{2}}{\pi} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)} \qquad \text{(eq. 21)}$$

In this application,

$$V_{ac,off} = \frac{0.7}{0.0123 \cdot \frac{2\sqrt{2}}{\pi} \cdot \left(1 - \frac{4.2\ Hz}{3 \cdot 50\ Hz}\right)} = 64.8\ Vac$$

which seems acceptable. By reducing C_{BO}, one can increase this level and vice versa. Note that this calculation result is just a reference since it doesn't include the voltage drop on the current loop, i.e. EMI filter and bridge diode etc.

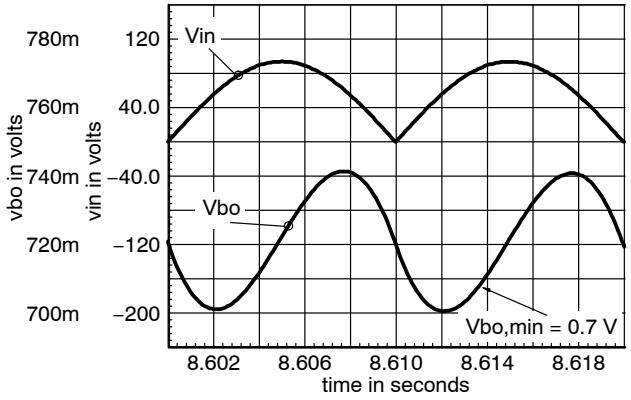

Figure 3. Ripple on V_{bo}

Finally

R_{boU1}	R_{boU2}	R_{boL}	C_{BO}
3.3 MΩ	3.3 MΩ	82.5 kΩ	0.47 μF

Step 4: Current Sense Network

The current sense circuitry consists of:

A current sense resistor R_{SENSE}.

A resistor R_{CS} that sets the current limit threshold.

A resistor R_M that adjusts the PFC stage power capability.

A capacitor C_M. CS pin sources a current, I_{cs}, that is proportional to the coil current. C_M must filter the coil current ripple so that I_{cs} is actually proportional to the input current, and makes the PFC stage operate at average current mode.

R_{SENSE}

Like with the NCP1653, you are free to implement the current sense resistor, R_{SENSE}, of your choice. Practically, losses considerations dictate its value. Once, you have selected the R_{SENSE} resistor without other constraint that the best trade off between losses and noise immunity, you just have to choose a second resistor R_{CS} to adjust the over−current threshold.

This flexibility in the current sense resistor, leads to a significant reduction of the losses. Practically, compared to circuits featuring a traditional constant 1 V over−current threshold, you can easily improve the efficiency of your PFC stage (up to almost 1%, in a wide mains application).

If one neglects the ripple current, maximum R_{SENSE} losses can be estimated by the following equation:

$$P_{R_{SENSE},max} = R_{SENSE} \cdot \left(\frac{P_{out,max}}{\eta \cdot V_{acLL}}\right)^2 \quad \text{(eq. 22)}$$

As a rule of the thumb, one can choose R_{SENSE} so that its dissipation does not exceed 0.5% of $P_{out,max}$. This criterion leads to

$$R_{SENSE} \leq 0.5\% \cdot \frac{(\eta \cdot V_{acLL})^2}{P_{out,max}} \quad \text{(eq. 23)}$$

In this application, solving of the precedent equation gives:

$$R_{SENSE} \leq 102\ m\Omega$$

Hence, 0.1 Ω is chosen as R_{SENSE} that would spend about 1.47 W.

R_{CS}

Simply select R_{CS} in order to set the desired over−current limit:

$$R_{CS} = \frac{R_{SENSE} \cdot I_{coil,max}}{I_{S(OCP)}} \quad \text{(eq. 24)}$$

where:

$I_{coil,max}$ is the maximum coil current

$I_{S(OCP)}$ is the internal over−current protection threshold (200 μA typical). To keep the design margin, it is recommended to use the minimum value of $I_{S(OCP)}$, 185 μA to design R_{CS}.

As the step 1 indicates that the maximum coil current is 6.4 A and R_{SENSE} is 0.1 Ω, R_{CS} is

$$\frac{0.1\ \Omega \cdot 6.4\ A}{185\ \mu A} = 3.46\ k\Omega$$

Choose 3.6 kΩ as R_{CS} as it is the closest higher normalized value in practical.

R_M and C_M

R_M adjusts the maximum power the PFC stage can supply given the chosen output voltage level. By choosing R_M high enough, you can force the "Follower Boost Operation" (Note 4). Use the following equation to select R_M:

$$R_M = 70\% \cdot \eta \frac{2\pi R_{CS} \cdot \Delta V_{CONTROL} \cdot V_{REF}}{\sqrt{2} R_{SENSE} K_{BO} V_{outLL} P_{out,max}} \cdot V_{acLL} \quad \text{(eq. 25)}$$

where:

- $\Delta V_{CONTROL}$ is the operating range of $V_{control}$ (3 V).
- V_{REF} is the internal voltage reference (2.5 V)
- V_{acLL} is the lowest level of the AC line rms voltage.
- $P_{out,max}$ is the maximum output power.
- η is the efficiency @ V_{acLL} and $P_{out,max}$.
- K_{BO} is the scale down factor betweenV_{in} and V_{BO},

$$\left(K_{BO} = \frac{R_{boL}}{R_{boU} + R_{boL}}\right)$$

- V_{outLL} is the output voltage corresponding to V_{acLL} in full load conditions. In traditional mode, V_{outLL} is the targeted regulation level (390 V in general). In Follower Boost, you can choose a lower value.
- 70% is to take into account the i_m dispersion.

Our application is a traditional one (constant output voltage). Hence, V_{outLL} equates 390 V and R_M is:

$$\frac{70\% \cdot 0.92 \cdot 2\pi \cdot 3.6\ k\Omega \cdot 3\ V \cdot 2.5\ V}{\sqrt{2} \cdot 0.1\ \Omega \cdot \frac{82.5\ k\Omega}{6.6\ M\Omega + 82.5\ k\Omega} \cdot 390\ V \cdot 300\ W} \cdot 85\ Vac$$

$$= 45.4\ k\Omega$$

Let's take a normalized 47 kΩ resistor as R_M.

For a correct filtering of I_{cs}, the time constant ($R_M \cdot C_M$) should be taken in the range of 5 times the operating cycle period, i.e. $5 \cdot 1/f_{sw}$. This time constant is large enough to filter the switching ripple and low enough not to distort the low frequency component, that is the 100 or 120 Hz rectified sinusoid.

In this application, 65 kHz operating frequency of NCP1654 is chosen, which operating cycle period is 15.4 μs. So the time constant ($R_M \cdot C_M$) should be in the range of 77 μs.

Hence

$$C_M \approx \frac{77\ \mu s}{R_M} = 1.6\ nF$$

Let's take C_M = 1 nF.

Finally

R_{SENSE}	R_{CS}	R_M	C_M
0.1 Ω	3.6 kΩ	47 kΩ	1 nF

4. The "Follower Boost" mode makes the pre−converter output voltage stabilize at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the difference between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage (refer to MC33260 and NCP1654 datasheet at www.onsemi.com).

CONSIDERATIONS REGARDING 200 kHz APPLICATIONS – DESIGN TIP AT HIGH LINE

By following above 4 steps, one can get the PFC converter done easily. However, there is a special situation needing the designer's care, which is when the input is at high line and the operating frequency is 200 kHz.

Please refer to Figures 5 and 4. As the operating frequency is 200 kHz and V_{out} is set at 390 V_{dc}, the input current is not smooth even at full load.

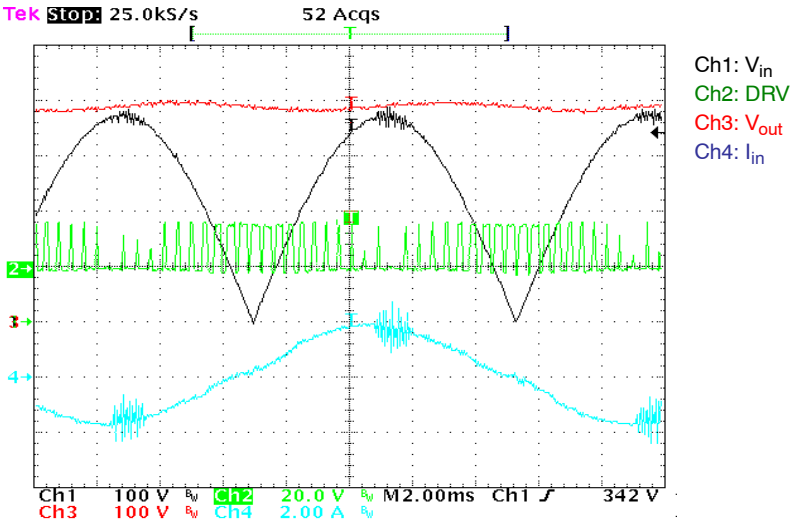

Figure 5. The Waveforms at 265 V_{ac}, 300 W as Controlled by 200 kHz NCP1654

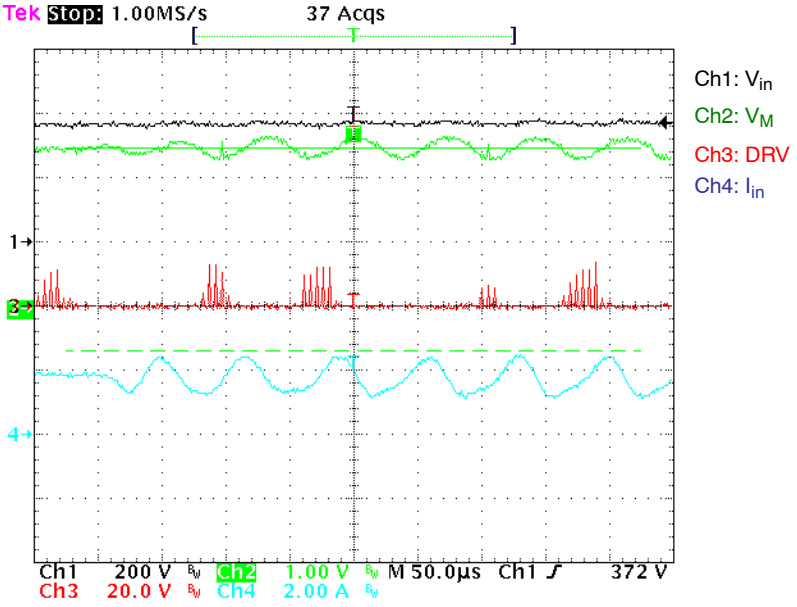

Figure 4. Zoom−in with Waveforms at Peak of 265 V_{ac}

As indicated in Figure 4, the PFC may operate at skip mode even at full load, which might produce audible noise.

The skip mode at peak of the sinusoidal 265 V_{ac} is caused by the fact that it exists several delay to turn off the power MOSFET, which include the propagation delay inside the controller, the turn−off delay of MOSFET itself, and the delay caused by driver circuit etc. Depending on the design, the delay to turn off MOSFET could be in the range of 0.2 µs to 0.4 µs.

If V_{out} is set at 390 V and the high line is 265 V_{ac}, which is the existing design for most of cases, then the duty at peak of the sinusoidal input is:

$$D = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{265 \cdot \sqrt{2}}{390} = 3.9\% \qquad \text{(eq. 26)}$$

When the operating frequency is 200 kHz, the on time at the peak of sinusoidal input is 0.2 μs. It is shorter than the total delay−off of MOSFET! In the end, PFC will go to the skip mode and might produce audible noise.

To solve the audible noise, there are 2 possible ways:

- Increase V_{out} and make the on time of MOSFET is above total delay−off of MOSFET.
  By solution 1, one can design the V_{out} by modifying the duty equation as follows:

$$V_{out} = \frac{V_{in}}{1 - D} = \frac{V_{in}}{1 \times t_{delay\_off} \cdot f_{op}} = \frac{265 \cdot \sqrt{2}}{1 - 0.4\,\mu \cdot 200k} = 407\ V \qquad \text{(eq. 27)}$$

  And then the PFC will keep operating continuously. The drawback of this solution is that there is less voltage margin concerning the bulk capacitor and the power devices.
- Modify the skip mode operation, which can help reducing the audible noise. Refer to Figure 6, the modified V_M pin structure. By inserting the R_{M2}, part of the ripple on the inductor current join the modulation of pulse width. It softens the skip mode operation reduces the audible noise.

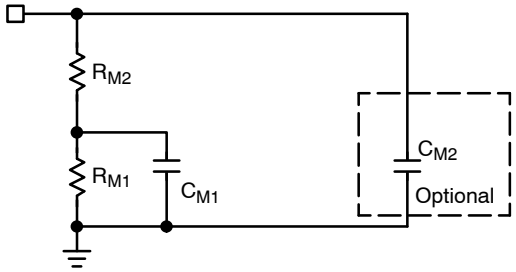

Figure 6. Modified V_M Pin Structure

The design steps of the modified V_M pin structure are proposed as follows:

1. Keep the total value of R_{M1} and R_{M2} equal to the original R_M value.
2. Trim R_{M2} value in the range of 20% to 100% of R_{M1} to adjust the skip mode performance at high line.
3. Add C_{M2} about 10% of C_{M1} for filtering the signal of V_M if needed.
4. Double check the performance at input ranging from 230 V_{ac} to high line.

Figure 7 shows the result after modification. It is denoted that there is still skip mode at peak of the sinusoidal input, but the audible noise is well−limited.

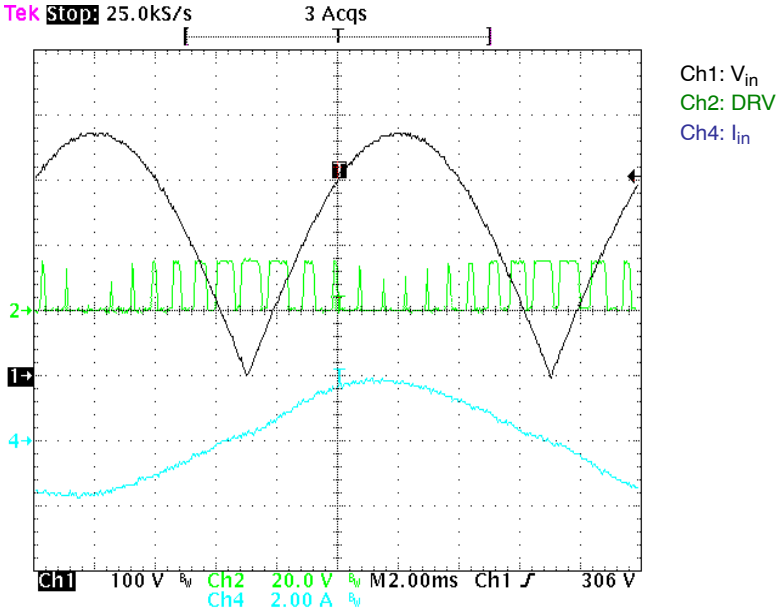

Figure 7. The Waveforms after Modifying the V_M Pin Structure

Summary

Steps	Components	Formula	300 W Application
Step 1: Coil Inductance, Bulk Capacitor and Power Silicon	Select the maximum switching peak to peak ripple of the coil current	Choose a value between 10 and 50% $\varrho = \frac{\Delta I_{coil,pp}}{I_{in,max}}$	ϱ = 36%
	Coil inductance (L)	$L = \frac{\eta \cdot V_{acLL}^{2}}{\varrho \cdot f_{sw} \cdot P_{out,max}} \left(1 - \frac{\sqrt{2} V_{acLL}}{V_{out}}\right)$	L = 650 μH
	Maximum rms coil current	$I_{coil,rms,max} = \frac{P_{out,max}}{\eta \cdot V_{acLL}}$	$I_{coil,rms,max}$ = 3.8 A
	Maximum coil current	$I_{coil,max} = \sqrt{2}\left(1 + \frac{\varrho}{2}\right)\frac{P_{out,max}}{\eta \cdot V_{acLL}}$	$I_{coil,max}$ = 6.4 A
	Bulk Capacitor (ripple voltage consideration)	$C_{bulk} > \frac{P_{out}}{\delta V_{pp,max} \cdot \omega \cdot V_{out}}$	180 μF / 450 V
	Bulk Capacitor (Hold up time consideration)	$C_{bulk} > \frac{2P_{out} \cdot t_{HOLD}}{V_{out1}^{2} - V_{out2}^{2}}$	
Step 2: Feedback Arrangement	$R_{fbU1} + R_{fbU2} + R_{fbL}$	$(R_{fbU1} + R_{fbU2}) = \frac{V_{out} - V_{REF}}{V_{REF}} R_{fbL}$	R_{fbL} = 23.2 kΩ R_{fbU1} = 1.8 MΩ R_{fbU2} = 1.8 MΩ
	C_{FB}	C_{FB} = 100 pF ~ 1 nF	C_{FB} = 100 pF
	C_P, C_Z, R_Z	$\frac{V_{control}}{V_{out}} = \frac{R_{fbL} \cdot G_{EA} R_Z}{R_{fbL} + R_{fbU}} \cdot \frac{1 + sR_ZC_Z}{sR_ZC_Z(1 + sR_ZC_P)}$	C_P = 0.22 μF C_Z = 2.2 μF R_Z = 12 kΩ
Step 3: Input Voltage Sensing	$R_{boU1} + R_{boU2} + R_{boL}$	$(R_{boU1} + R_{boU2}) = \frac{\sqrt{2} V_{ac,on} - V_{BOH}}{V_{BOH}} R_{boL}$	$V_{ac,on}$ = 75 Vac R_{boL} = 82.5 kΩ R_{boU1} = 3.3 MΩ R_{boU2} = 3.3 MΩ
	C_{BO}	$C_{BO} \approx \frac{5 \cdot T_{Vin}}{R_{boL}}$	C_{BO} = 0.47 μF
Step 4: Current Sense Network	R_{SENSE}	Choose R_{SENSE} so that its dissipation keeps reasonable, e.g. select R_{SENSE} so that P_{Rsense} is less than 0.5% · $P_{out,max}$. $R_{SENSE} \leq 0.5\% \cdot \frac{(\eta \cdot V_{acLL})^2}{P_{out,max}}$	R_{SENSE} = 0.1 Ω / 3 W
	R_{CS}	$R_{CS} = \frac{R_{SENSE} \cdot I_{coil,max}}{185\ \mu A}$	R_{CS} = 3.6 kΩ
	R_M	$R_M = 70\% \cdot \eta \frac{2\pi R_{CS} \cdot \Delta V_{CONTROL} \cdot V_{REF}}{\sqrt{2} R_{SENSE} K_{BO} V_{outLL} P_{out,max}} \cdot V_{acLL}$	R_M = 47 kΩ
	C_M	$C_M \approx 5 \cdot \frac{1}{R_M f_{sw}}$	C_M = 1 nF

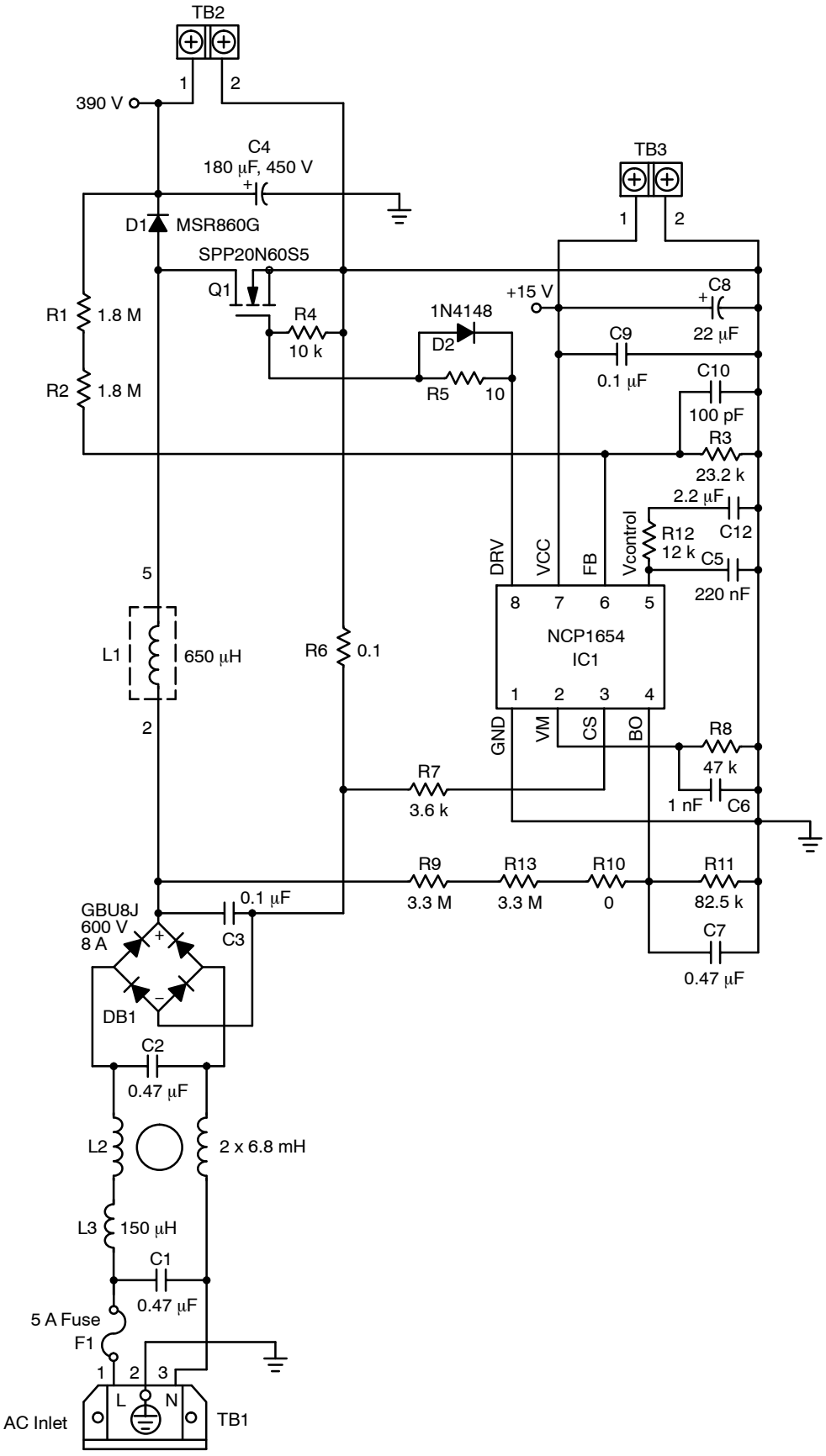

Figure 8. 300 W Application Schematic

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